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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/646,681	08/21/2003	Ryan Lei	42P16687	1018

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EXAMINER	
ISAAC, STANETTA D	
ART UNIT	**PAPER NUMBER**
2812	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/646,681	LEI ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,7,9-12,14,15,19-25,27,28,30 and 33-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,7,9-12,14,15,19-25,27,28,30 and 33-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed on1/10/07. Currently, claims 1, 3, 4, 7, 9-12, 14, 15, 19-25, 27, 28, 30 and 33-49 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The rejection of claims 1, 3, 7, 9-12, 14, 19-25, 27, and 30 under 35 U.S.C. 102(b) as being anticipated by Reisman et al., US Patent 4,891,329 has been maintained for reasons of record.

Reisman discloses the semiconductor method as claimed. See figures 1A-1D, and corresponding text, where Reisman teaches, pertaining to claims 1, 12 and 22, a method of forming a germanium-on-insulator (GOI) substrate comprising: forming an epitaxial germanium layer **20** on top of a first substrate **10** (the epitaxial germanium layer having a rough surface, the rough surface has a roughness value approximately greater than 2nm RMS, for claim 12; figure 1A; col. 4, lines 21-30, ***Note***: the Examiner takes the position that it is inherent the rough surface has a roughness value approximately greater than 2nm RMS, based on Applicant's admitted prior art on page 6, paragraph [0019]); forming a first dielectric film **30** on top of the epitaxial germanium layer (on top of the rough surface, for claim 12; figure 1B; col. 4, lines 30-33); providing a second semiconductor substrate comprising a semiconductor surface **40/50** (figure

1C; col. 4, lines 54-59, ***Note***: the Examiner takes the position that the second semiconductor substrate comprises both the insulating layer and the second substrate); bonding the first substrate directly to the second substrate by bonding the first dielectric film to the semiconductor surface second substrate, the bonding resulted in a bonded wafer pair (figure 1C; col. 4, lines 60-65); and removing the first substrate after the bonding to expose epitaxial germanium layer to form the GOI substrate (and forming an electronic device on the GOI substrate, for claim 22; figure 1D; col. 4, lines 66-68; col. 5, lines 1-2; col. 6, lines 52-55).

Pertaining to claims 3, 14 and 27, Reisman teaches, a method, wherein the removing of the first substrate after the bonding includes one of a grind back process, an etching process, and an ion exfoliation process (figure 1D; col. 4, lines 66-68).

Pertaining to claims 7 and 30, Reisman teaches, a method wherein the removing of the first substrate after the bonding includes cleaving off the first substrate (figure 1D; col. 4, lines 66-68).

Pertaining to claims 9 and 19, Reisman teaches, a method wherein each of the first substrate and the second substrate semiconductor wafer is selected from a group consisting of a silicon (Si) substrate, a monocrystalline Si substrate, a polycrystalline Si substrate, a Si-containing substrate, a Si substrate having an oxide layer, a silicon-on-insulator (SOI) substrate, a gallium arsenide substrate, and Ge-containing substrate (col. 4, lines 22-25 and lines 54-56, both the first substrate and second substrates are silicon).

Pertaining to claims 10 and 20, Reisman teaches, a method further comprising causing a surface activation to the top surface of the first dielectric film and at least one surface of the second substrate to facilitate the bonding (col. 4, lines 60-65).

Pertaining to claims 11 and 21, Reisman teaches, a method further comprises annealing the bonded wafer pair at a predetermined annealing temperature, wherein the annealing temperature is achieved with a temperature ramp rate of approximately 1°C/minute (col. 4, lines 64-65).

Pertaining to claim 23, Reisman teaches, a method wherein the electronic device includes one of a transistor and a detector (col. 1, lines 5-12; col. 6, lines 52-55).

Pertaining to claim 24, Reisman teaches, a method wherein the transistor includes a gate dielectric, a gate electrode, spacers, and source/drain regions (col. 1, lines 5-12; col. 6, lines 52-55).

Pertaining to claim 25, Reisman teaches, a method wherein the detector includes a waveguide encapsulated by an oxide layer and at least one electrode (col.1, lines 1-12; col. 6, lines 52-55).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The rejection of claims 4, 15, 28, 33, 39, and 44 under 35 U.S.C. 103(a) as being unpatentable over Reisman et al., US Patent 4,891,329 in view of admitted prior art has been maintained for reasons of record.

Reisman disclose the semiconductor method substantially as claimed. See preceding rejection of claims 1, 3, 7, 9-12, 14, 19-25, 27, and 30 under 35 U.S.C. 102(e). In addition, Riesman shows, pertaining to claims 33, 39 and 44, a method of forming a germanium-on-insulator (GOI) substrate comprising: forming an epitaxial germanium layer **20** on top of a first substrate **10** (the epitaxial germanium layer having a rough surface, the rough surface has a roughness value approximately greater than 2nm RMS, for claim 39; figure 1A; col. 4, lines 21-30, ***Note***: the Examiner takes the position that it is inherent the rough surface has a roughness value approximately greater than 2nm RMS, based on Applicant's admitted prior art on page 6, paragraph [0019]); forming a first dielectric film **30** on top of the epitaxial germanium layer (on top of the rough surface, for claim 12; figure 1B; col. 4, lines 30-33); providing a second semiconductor substrate **40/50** (figure 1C; col. 4, lines 54-59, ***Note***: the Examiner takes the position that the second semiconductor substrate comprises both the insulating layer and the second substrate); bonding the first substrate directly to the second substrate by bonding the first dielectric film to the second substrate, the bonding resulted in a bonded wafer pair (figure 1C; col. 4, lines 60-65); and removing the first substrate after the bonding to expose epitaxial germanium layer to form the GOI substrate (and forming an electronic device on the GOI substrate, for claim 22; figure 1D; col. 4, lines 66-68; col. 5, lines 1-2; col. 6, lines 52-55). In addition, Riesman shows, pertaining to claims 34, 40 and 48, wherein the removing of the first substrate after the bonding includes one of a grind back process, an etching process, and an ion exfoliation process (figure 1D; col. 4, lines 66-68). Also, Riesman shows, pertaining claims, 35 and 49, wherein the removing of the first substrate after the bonding includes cleaving off the first substrate (figure 1D; col. 4, lines 66-68). Riesman shows, pertaining to claims 36 and 41,

wherein each of the first substrate and the second substrate semiconductor wafer is selected from a group consisting of a silicon (Si) substrate, a monocrystalline Si substrate, a polycrystalline Si substrate, a Si-containing substrate, a Si substrate having an oxide layer, a silicon-on-insulator (SOI) substrate, a gallium arsenide substrate, and Ge-containing substrate (col. 4, lines 22-25 and lines 54-56, both the first substrate and second substrates are silicon). In addition, Riesman shows, pertaining to claims 37 and 42, method further comprising causing a surface activation to the top surface of the first dielectric film and at least one surface of the second substrate to facilitate the bonding (col. 4, lines 60-65). Also, Riesman shows, pertaining to claims 38 and 43, further comprises annealing the bonded wafer pair at a predetermined annealing temperature, wherein the annealing temperature is achieved with a temperature ramp rate of approximately 1°C/minute (col. 4, lines 64-65). Riesman shows, pertaining to claim 45, wherein the electronic device includes one of a transistor and a detector (col. 1, lines 5-12; col. 6, lines 52-55). In addition, Reisman shows, pertaining to claim 46, wherein the transistor includes a gate dielectric, a gate electrode, spacers, and source/drain regions (col. 1, lines 5-12; col. 6, lines 52-55). Finally, Reisman shows, pertaining to claim, 47, wherein the detector includes a waveguide encapsulated by an oxide layer and at least one electrode (col.1, lines 1-12; col. 6, lines 52-55).

However, Reisman fails to show, pertaining to claims 4, 15, 28, 33, 39 and 44, further comprising: polishing the surface of the first dielectric film prior to the bonding.

On page 8, paragraph [0025], the Applicant teaches, that portions of the dielectric layer, can be removed to have a smaller thickness, where a conventional method of chemical mechanical polishing (CMP) may be used to remove some of the dielectric layer.

It would have been obvious to one of ordinary skill in the art to incorporate, a method further comprising: polishing the surface of the first dielectric film prior to the bonding, in the method of Reisman, pertaining to claims 4, 15 and 28, according to the teachings of the admitted prior art, with the motivation of, reducing the amount of dielectric material, for the purpose of creating a desired dielectric thickness.

Response to Arguments

Applicant's arguments filed 1/10/07 have been fully considered but they are not persuasive. The Applicant raises the clear issue as to whether Riesman alone or in combination thereof, suggest bonding the insulator layer of the first substrate directly to the semiconductor surface second semiconductor substrate. In addition, Applicant raises the clear issue as to whether Riesman alone or in combination thereof, suggest depositing a dielectric film sufficiently thick to cover the surface roughness of the underlying germanium layer.

The Examiner takes the position that Riesman does suggest bonding the insulator layer of the first substrate directly to the surface of the second semiconductor substrate. Specifically, "comprising a semiconductor surface", taken in its broadest interpretation, does not preclude surface layers between the surface of the semiconductor substrate, where Riesman meets this limitation, by showing the step of bonding the first substrate **10** directly to the second substrate **40/50** (the second semiconductor substrate includes both the insulating layer and the substrate) bonding the first dielectric film **30** to the second substrate, the bonding resulted in a bonded wafer pair (figure 1C; col. 4, lines 60-65). With regards to the dielectric film being sufficiently thick to cover the surface roughness of the epitaxial layer, the Applicant fails to define any quantitative amounts or degrees of similarity to the claim language that would thereby limit the

scope of the term "sufficiently thick". Therefore, the Examiner takes the position that Riesman does discloses, in the claims broadest interpretation a "sufficiently thick" dielectric layer that covers the epitaxial layer.

Conclusion

1. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stanetta Isaac
Patent Examiner
April 1, 2007

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER